Research Article | Vol. 28, No. 22 / 26 October 2020 / Optics Express 32793
Optics EXPRESS

Micro-transfer-printed III-V-on-silicon C-band distributed feedback lasers

BAHAWAL HAQ,[1,2,*] JAVAD RAHIMI VASKASI,[1,2] JING ZHANG,[1,2] AGNIESZKA GOCALINSKA,[3] EMANUELE PELUCCHI,[3] BRIAN CORBETT,[3] AND GUNTHER ROELKENS[1,2]

[1] *Photonics Research Group, Ghent University-IMEC, 9052 Ghent, Belgium*
[2] *Center for Nano- and Biophotonics, Ghent University, Ghent, Belgium*
[3] *Tyndall National Institute, University College Cork, Lee Maltings, Cork, Ireland*
[*] *bahawal.haq@ugent.be*

Abstract: We report on single-mode C-band distributed feedback lasers fabricated through micro-transfer-printing of semiconductor optical amplifier coupons fabricated on a InP source wafer onto a silicon-on-insulator photonic circuit. The coupons are micro-transfer printed on quarter-wave shifted gratings defined in SiN deposited on the silicon waveguide. Alignment-tolerant adiabatic tapers are used to efficiently couple light from the hybrid III-V/Si waveguide to the Si waveguide circuit. 80 mA threshold current and a maximum single-sided waveguide-coupled output power above 6.9 mW is obtained at 20 °C. Single mode operation around 1558 nm with > 33 dB side mode suppression ratio is demonstrated. Micro-transfer printing-based heterogeneous integration is promising for the wafer-level integration of advanced laser sources on complex silicon photonic integrated circuit platforms without changing the foundry process flow.

1. Introduction

Photonic integrated circuits (PICs) are currently being utilized mostly in telecom and datacom markets [1]. Recently, various sensing products based on PICs have also been introduced in the market. The realization of aformentioned products are based on the smaller form-factor, the lower fabrication cost due to wafer-level high-volume production, and the wide range of functionalities PICs can offer [2,3]. Silicon photonics (SiPh) offers an added advantage as it can utilize the acquired knowledge and massive infrastructure developed for electronics IC fabrication over the last decades. Today, there are several CMOS-fabs around the world with a mature process flow for SiPh PICs [4].

However, wafer-level and high-density integration of lasers and semiconductor optical amplifiers on a silicon photonics platform is still a bottleneck. This is a hindrance in the development of advanced SiPh systems-on-chip. Several approaches are being developed to overcome this problem, ranging from the flip-chip integration of III-V opto-electronic devices over III-V die-to-wafer/wafer-to-wafer bonding to hetero-epitaxial growth. Front-end hetero-epitaxial growth of III-V semiconductors represents the ultimate path to integrate light sources on silicon photonics and proof-of-concept devices have been demonstrated, but many technological hurdles need to be overcome before this becomes a viable technology [5]. In the case of flip-chip integration mature III-V technology can be used and with efficient optical coupling devices such as semiconductor optical amplifiers (SOAs) can be realized. Testing the devices on the source wafer prior to integration is possible, but the sequential assembly (using active or passive alignment) can be a bottleneck and double-sided coupling is difficult for III-V chips with a cleaving tolerance of several micrometer [6].

The die-to-wafer bonding approach has the advantage of high throughput integration: with die-to-wafer bonding unstructured III-V dies are bonded epi-side down to a silicon photonic

#404847 https://doi.org/10.1364/OE.404847
Journal © 2020 Received 7 Aug 2020; revised 5 Oct 2020; accepted 7 Oct 2020; published 15 Oct 2020

Optics EXPRESS

wafer. The unpatterned dies do not need accurate alignment, making this a high-throughput approach. After bonding and III-V substrate removal the III-V epitaxial layers can be processed on wafer-scale, lithographically aligned to the underlying Si waveguides, thus removing the need for active alignment. Several high-performance III-V-on-Si hybrid lasers with more than 10 mW output power and higher operating temperature of above 70 ^{o}C have been demonstrated with III-V die-to-wafer bonding [3,7]. While this enables dense integration of efficient light sources and optical amplifiers, the SiPh back-end flow needs to be modified for the III-V integration [8–10]. Moreover, this approach doesn't allow dense integration of devices based on a different III-V epitaxial structure on the SiPh circuits, given the minimum die size of a few mm that can easily be handled and processed. Therefore, there is a need for an alternative approach that combines the advantages of flip-chip integration (processing of III-V devices on the III-V source wafer, pre-testing) and die-to-wafer bonding (high throughput integration, straightforward integration of waveguide-in/waveguide-out devices). In this paper, we integrate distributed feedback (DFB) lasers on silicon photonic integrated circuits containing quarter-wave shifted gratings based on the micro-transfer-printing of III-V SOA coupons fully processed on an InP source wafer.

2. Micro-transfer-printing technology

Micro-transfer-printing technology takes advantage of the visco-elastic effect in poly-dimethyl-siloxane (PDMS). The adhesion of the PDMS stamp to the SOA coupon depends on the velocity by which the stamp is removed. The coupons are picked-up with higher velocity and printed (delaminated from the stamp) by slowly retracting the PDMS stamp. Higher velocity produces stronger adhesive force to pick the coupons (by breaking the tether structures that keep the coupons in place) and using a lower velocity with an additional shear force prints the devices on the target site [11]. Several heterogeneously integrated photonic devices have been demonstrated using micro-transfer-printing technology [12–14]. The process starts with the definition of the III-V opto-electronic components on a III-V source wafer, which has the active epitaxial layer stack grown on top of a release layer (*i.e.* InGaAs or InAlAs for the InP material system). After patterning of the device and the release layer, the structures are encapsulated and anchored to the substrate by this encapsulation and the release layer is selectively removed using FeCl3:H2O wet etching, keeping the III-V components in place through the anchoring. With the PDMS stamp, one or more thin-film III-V components can be picked up from the III-V source wafer and printed on an SOI target wafer. Then, the encapsulation is removed with a dry etching process and the III-V devices are electrically contacted on wafer level. This approach enables pretesting of the III-V devices on the III-V source wafer, similar to flip-chip integration, but also it enables massively parallel integration, similar to the die-to-wafer bonding approach. The III-V devices are micro-scale, so the SiPh back-end flow does not need to modified to accommodate the III-V devices. Only a local opening to the Si device layer is needed, similar to the flip-chip integration approach. The III-V material is used in an efficient way as the bondpads to the devices - which occupy the most space in classical III-V opto-electronic devices, are realized on the target wafer, not on the source wafer. Because micro-scale devices are transfer printed, different III-V devices, potentially from different III-V epitaxial wafers can be intimately integrated on a PIC.

3. Design of the III-V-on-silicon distributed feedback laser

The silicon waveguide platform consists of a 400 nm thick Si device layer on a 2 μm thick buried oxide (BOX). The Si waveguide in the gain section of the DFB laser is 2.0 μm wide and has a 20 nm etch depth. It is defined by etching 3.0 μm wide trenches. 50 nm PECVD SiN is deposited and etched periodically on the top of the Si waveguide to define the quarter-phase shift grating. The design schematic and the longitudinal cross section are illustrated in Fig. 1.One of the major issues when micro-transfer-printing a processed SOA is the stringent alignment requirement between III-V and Si waveguide required for efficient coupling of light from the III-V to Si

Optics EXPRESS

waveguide. Efficient coupling can be achieved by designing an alignment tolerant adiabatic taper as discussed in [13]. 1 μm alignment tolerance is achieved, when the alignment tolerant adiabatic taper is micro-transfer-printed on a 3.0 μm wide silicon waveguide. Reducing the width of the III-V and Si waveguide has an adverse effect on the alignment tolerance of the adiabatic taper and can result in a deterioration of the slope efficiency of the DFB laser. However, a 3.0 um wide Si and III-V waveguide in the gain section supports multiple transverse modes that appear in the output spectrum of the DFB laser. One way to solve this multi-mode problem is to do ion implantation on the edges of III-V mesa during III-V SOA processing, as demonstrated by UCSB, Intel and Aurrion [3,15]. This results in low resistance path in the center and high resistance path at the edges of the mesa, thus, increasing the overlap of the carriers with the fundamental mode. However, in this paper a different approach has been followed. The etch-depth and the width of the Si waveguide is set to 20 nm and 2.0 μm. This reduces the number of transverse modes in the gain section without adversely affecting the alignment tolerance of the adiabatic taper which is important for micro-transfer-printing of processed SOAs. Moreover, reducing the etch-depth of the Si waveguide to 20 nm in the gain section increases the confinement factor of the optical mode in the Si waveguide which improves the internal loss in the DFB laser. However, this also means that defining grating in the Si will produce high κ gratings resulting in high κL DFB laser.

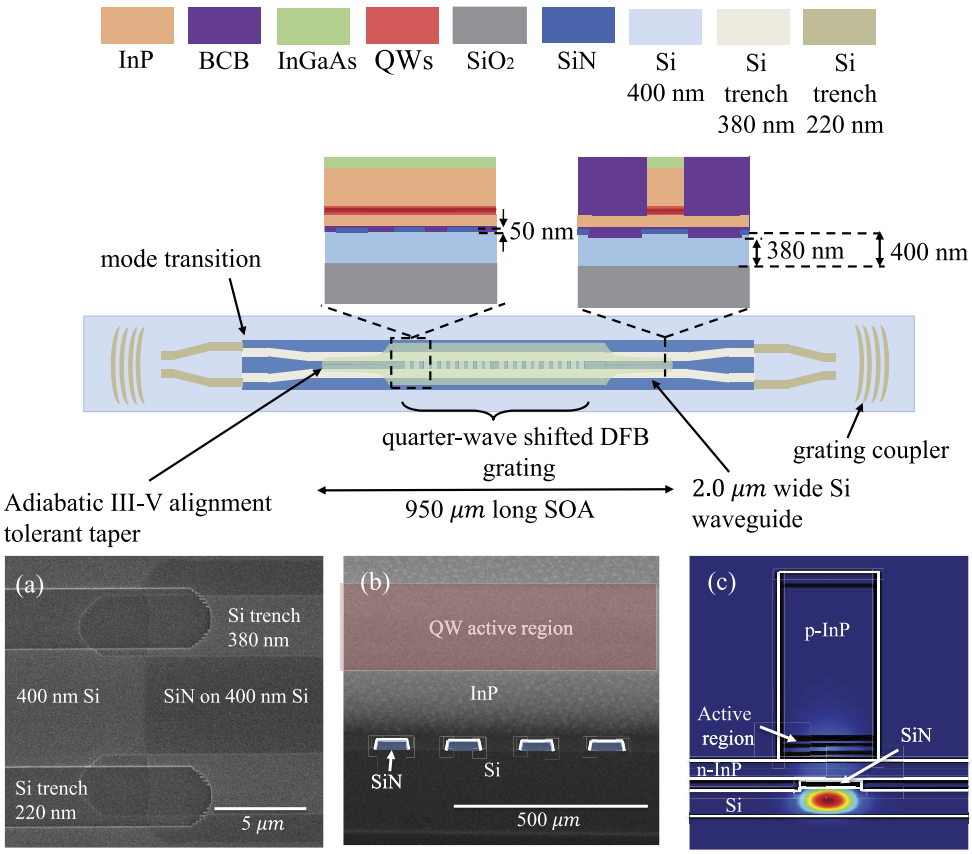

Fig. 1. Schematic illustrating the design of the DFB laser with cross-section view of the adiabatic taper and the side view of the DFB grating. SEM images of a) mode transition, b) longitudinal cross section of the DFB grating and c) the mode profile in the gain section are also shown.

Optics EXPRESS

In order to de-couple the dependence of internal loss and κL, the grating is patterned on a 50 nm PECVD SiN layer deposited on the top of the Si waveguide. This can lower the internal loss in the DFB cavity without increasing the κL of the grating for the same length of the SOA. The slope efficiency of the DFB laser is inversely proportional to the internal loss for a given κL, therefore, lower internal loss can result in higher slope efficiency.

The mode profile is shown in Fig. 1(c). The confinement of the mode in the multi-quantum wells in the active region (consisting of 6 quantum wells) is calculated using mode solver to be 2.1 percent. This is relatively low due to the higher refractive index of the shallow etch Si waveguide in the gain section. The SOA micro-transfer-printed on the Si waveguide consists of two alignment-tolerant adiabatic tapers, discussed in detail in [13], that are 224 μm long and a straight gain waveguide section which is 3.2 μm wide and 500 μm long. The adiabatic taper narrows down from 3.2 μm to 0.6 μm width. It is designed to overcome the coupling losses due to the lateral misalignment of the III-V mesa with respect to the silicon waveguide, inherent to the transfer printing integration method. The calculated coupling loss is 0.2 dB at 0.6 μm misalignment, when micro-transfer-printed on a 2.0 μm wide Si waveguide. The DFB laser is interfaced with a single-mode optical fiber by coupling the optical mode from a 20 nm etch-depth Si waveguide to a 180 nm etch-depth Si waveguide using a mode converter, which is connected to a 180 nm etched grating coupler.

The III-V epitaxial layer structure used in this work is described in detail in [13]. It consists of a 200 nm thick highly-doped p-InGaAs contact layer, a 1.5 μm thick p-InP cladding, a 25 nm thick InGaAsP etch stop layer, a pair of 40 nm thick AlInGaAs transition layers separating the InP cladding layers from the separate confinement heterostructure (SCH) layers, a pair of 75 nm thick AlGaInAs SCH layers, an active region with 6 AlInGaAs quantum wells sandwiched between AlInGaAs barriers (C-band gain spectrum), a 200 nm thick n-InP contact layer with 60 nm thick intrinsic InP layer underneath and a 50 nm/500 nm thick InGaAs/AlInAs release layer grown on the InP substrate.

4. Device fabrication

4.1. Processing of SOAs on InP substrate

The fabrication begins with the patterning of the SOA and the release layer. These SOA coupons are fabricated in a dense array on the III-V source wafer with a vertical pitch of 90 μm pitch. The length of the coupons is 950 μm and their width is 45 μm in this work. First step in the SOA processing is the etching of the protective thin InP layer on top of the p-InGaAs contact. It is removed by wet-etching in HCl. This is followed by the deposition of a SiN hardmask and standard i-line optical lithography is used to pattern the hardmask. The mesa is formed with a dry etching process and it is also briefly etched in the diluted HCl to make it V-shaped, as shown in Fig. 2. After this, SiN is deposited again to passivate the side-walls of the mesa. The active region is then etched using a combination of dry and wet-etching. Subsequently, a lift-off process is used to deposit the Ni/Ge/Au/Ti/Au n-contact and the device is passivated with SiN and BCB. With a similar lift-off process Ti/Au is deposited for the p-contact. The coupon boundary is then patterned and etched using a dry etching process. This ends the processing of the III-V SOA, however, for under-etching the device so that it can be picked-up by the PDMS stamp, the release layer is patterned and tethers are formed and anchored to the InP substrate as shown in Fig. 2(b-c). The SOA processing is described more in detail in [13]. An aqueous $FeCl_3$ solution at 7 ^{o}C is used to under-etch the InGaAs/AlInAs release layer. It takes 45 mins to release the 45 μm wide coupons. The coupons during and after the release layer etch are supported by the photo-resist tethers anchored to the InP substrate, as shown in Fig. 2(d).

Optics EXPRESS

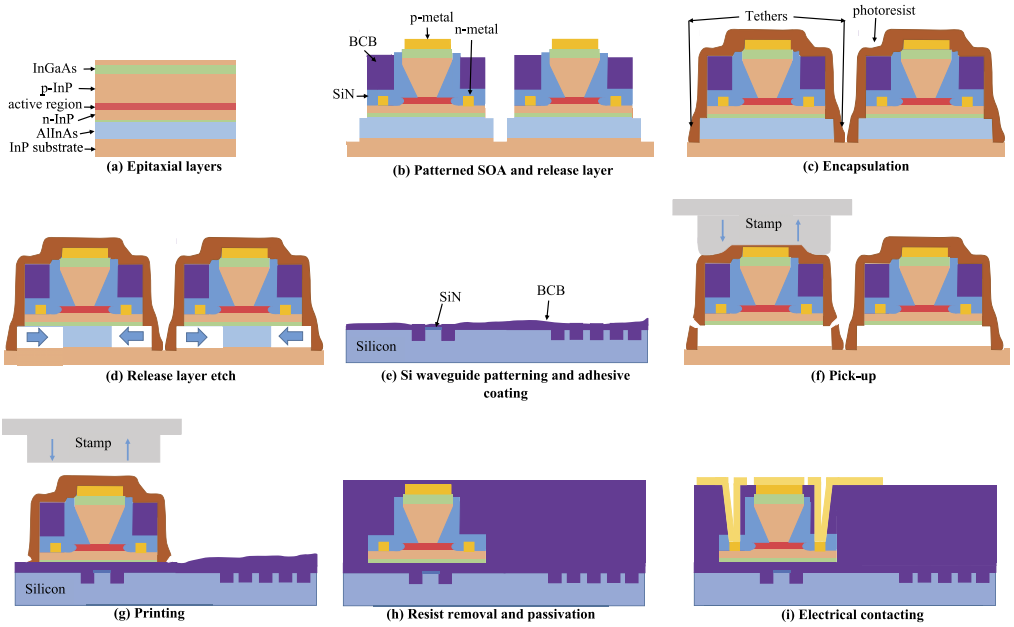

Fig. 2. Schematic fabrication process flow of micro-transfer printed III-V-on-Si DFB lasers, (a-d) depicts the processing of SOAs on the InP substrate, (e) illustrates the preparation of the patterened SiPh sample prior to micro-transfer-printing, (f-g) illustrates the picking and printing of the SOAs on the SiPh sample, (h-i) illustrates the post-processing steps on the SiPh sample which includes passivation and electrical contacting.

4.2. Micro-transfer-printing process

The micro-transfer printing process is illustrated in Fig. 2(e-i). The SiPh sample is first prepared for the micro-transfer-printing. Firstly, a 1:4 DVS-BCB-35:Mesitylene solution is spin coated on the sample as an adhesive bonding layer. A PDMS stamp with a 1000×50 μm^2 post size is used for the micro-transfer printing using an X-Celeprint μTP-100 tool. The SOA coupons are picked sequentially from the III-V source sample and pattern recognition is used to align them to the target Si waveguide structure. There are alignment markers on the SOA coupons and on the side of the Si waveguides. The μTP-100 tool software recognizes the markers and finds their center which is then aligned in the lateral and vertical directions by moving the SiPh target sample. After the alignment process is completed, the SOA coupon is pressed on the target sample and shear force is applied to detach the laminated coupon from the stamp. The stamp then slowly moves upward from the target, leaving the SOA attached to the silicon photonic target waveguide structure.

After printing all the SOA coupons, a dry etching process is used to remove the photo-resist encapsulation and the DVS-BCB is fully cured at 270 ^{o}C. The SiPh chips are then passivated with a thick DVS-BCB layer as shown in Fig. 2(h). Vias are patterned with i-line optical lithography and are defined using dry etching. Finally, 40nm/700nm Ti/Au is deposited through a lift-off process to define contact pads as illustrated in Fig. 2(i).

Figure 3 shows microscope pictures during the device processing. Figure 3(a) shows a dense array of SOAs fabricated on the InP source wafer. A zoom-in on a single SOA coupon is shown in Fig. 3(b), illustrating the metallized III-V waveguide, alignment markers used during the micro-transfer printing process and the tethers holding the devices in place on the InP substrate during and after the release etch. Figure 3(c) shows a microscope image of micro-transfer-printed

Optics EXPRESS

coupons on the SiPh waveguide circuit. Figure 3(d) shows a microscope image of the final sample with contact pads.

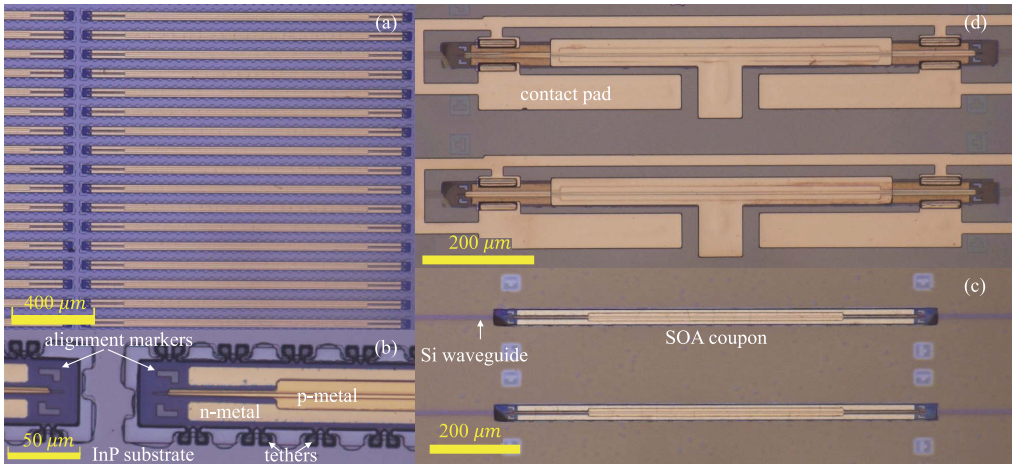

Fig. 3. (a) Microscope image of an array of SOA coupons on the InP source substrate, (b) Zoomed-in image of SOA coupons after release layer etch, (c) micro-transfer-printed SOA coupons on the SiPh circuit, (d) DFB laser chip after contact metal deposition.

5. Device Characterization

The DFB characterized in this paper has a 490 μm long grating. The grating period and duty cycle is 242 nm and 50 percent, respectively. The DFB sample is placed on a temperature controlled stage to characterize it. Single-mode cleaved fibers are used as an optical interface. The optical power couples from the grating coupling to a single-mode optical fiber which is connected to an optical spectrum analyzer and to an optical power meter. A Keithley 2400 Sourcemeter is used to bias the DFB laser. In order to calculate the on-chip optical power, reference waveguides with waveguide transitions and grating couplers are also fabricated on the same sample. The loss from the grating coupler and the mode transition is calibrated out to calculate the on-chip power. At 1558 nm, single-sided PIC to fiber coupling loss is 12.3 dB. This is consistent with the grating coupler loss reported in [13].

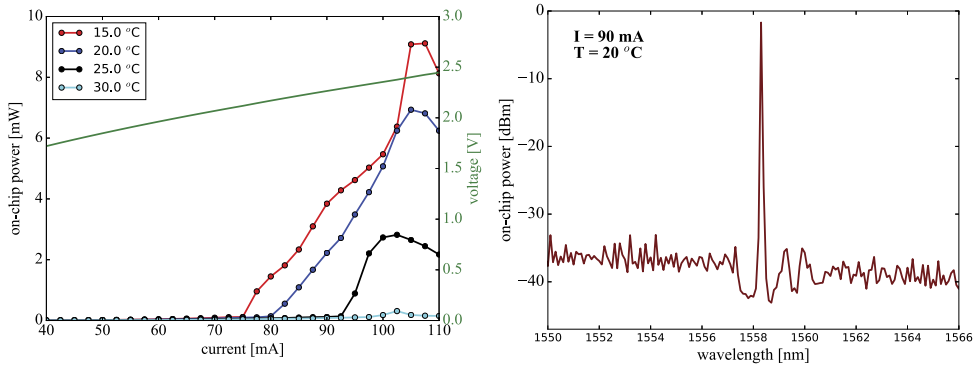

Fig. 4. (left) waveguide-coupled output power (single-sided) as a function of bias current for various operating temperatures and the current-voltage characteristic, (right) Measured spectrum at 0.05 nm resolution, at 90 mA and at 20 ^{o}C operating temperature.

Optics EXPRESS

The differential series resistance of the laser is 8.0 Ω. Figure 4(left) shows the LI curve for the DFB laser at various operating temperatures. Single-side waveguide coupled optical power of 9.1 mW, 6.9 mW and 2.8 mW is obtained at 15 °C, 20 °C and 25 °C, respectively. The threshold current at 20 °C is 80 mA and increases with the increase in operating temperature. The slope efficiency is calculated to be 0.27 W/A at 20 °C. Single mode operation at 1558.3 nm (resolution of 0.05 nm) with a side mode suppression better than 33 dB is obtained at 90 mA, shown in Fig. 4(right). The stop band is 2 nm wide which corresponds to κL of 2.6. Figure 5(left) and Fig. 6(left) shows the tunability of the DFB laser with the changing bias current. It tunes up to 0.4 nm when the bias current is varied from 80 mA to 110 mA and has a tuning coefficient of 0.0135 nm/mA, calculated by fitting a curve to the measured data. 1.4 nm red shift is obtained in the emission wavelength when operating temperature increases from 15 °C to 30 °C, resulting in temperature coefficient of 0.09 nm/°C. Due to relatively low confinement in the QWs and high thermal impedance, the maximum operating temperature of these lasers is relatively low as compared to the state-of-the-art DFB lasers demonstrated [3]. However, the thermal impedance of this design can be improved by incorporating thermal vias between the laser and silicon substrate (e.g. using amorphous silicon or metal). Alternatively, the chip can be mounted up-side down on a carrier that also acts as a good heat spreader (i.e. AlN carrier). In the current configuration the DFB laser is supposed to be used under cooled conditions, as the performance is only sufficient till 20 °C. This implies use outside the field of datacom, e.g. for silicon photonic sensor applications.

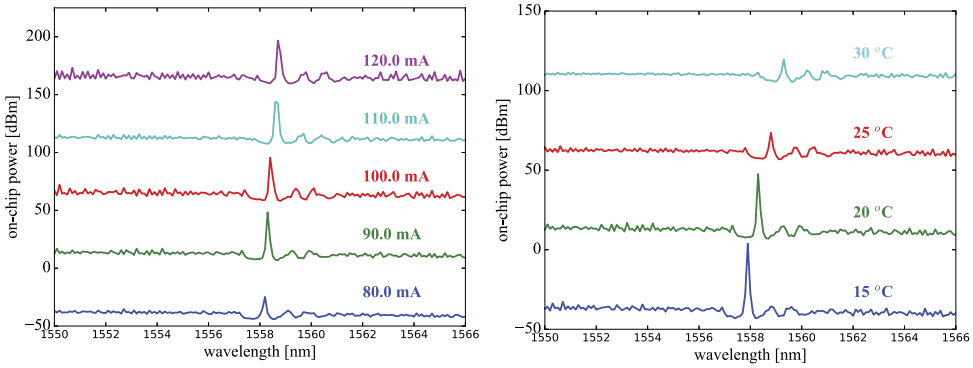

Fig. 5. Measured laser spectra (left) for various bias currents at 20 °C and (right) for various operating temperatures at 90 mA bias current, plotted with a 50 dB offset in the y-direction.

Optics EXPRESS

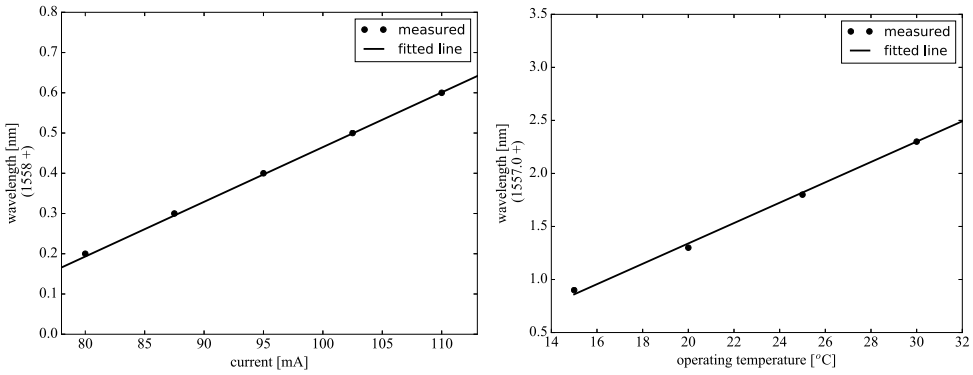

Fig. 6. DFB ouput wavelength tuning characteristics (left) with changing bias current at 20 ^{o}C and (right) with changing operating temperature at 90 mA.

6. Conclusion

We report the fabrication of a single-mode III-V-on-silicon DFB laser by micro-transfer-printing a processed SOA on the SiPh circuit. We report maximum output power of 9.1 mW at 15 ^{o}C, threshold current of 80 mA and slope efficiency of 0.27 W/A at 20 ^{o}C. This heterogeneous integration approach allows for wafer-scale integration of III-V opto-electronic components on a complex SiPh foundry platform.

Funding

INTERREG-fwvl SAFESIDE; H2020 TOPHIT; Science Foundation Ireland (12/RC/2276, 12/RC/2276-P2).

Acknowledgments

The authors would like to thank Liesbet Van Landschoot for the FIB cross-sections and Muhammad Muneeb for assistance related to fabrication and processing.

Disclosures

The authors declare no conflicts of interest.

References

1. Q. Cheng, M. Bahadori, M. Glick, S. Rumley, and K. Bergman, "Recent advances in optical technologies for data centers: a review," Optica **5**(11), 1354–1370 (2018).
2. "Infinera PICs," https://www.infinera.com/innovation/photonic-integrated-circuit.
3. H. Yu, J. Doylend, W. Lin, K. Nguyen, W. Liu, D. Gold, A. Dahal, C. Jan, R. Herrick, G. A. Ghiurcan, S. R. Hollingsworth, R. T. Romero, M. E. Favaro, L. Qiu, D. Zhu, and Y. Akulova, "100Gbps CWDM4 silicon photonics transmitter for 5G applications," in *2019 Optical Fiber Communications Conference and Exhibition (OFC)*, (2019).
4. A. Rahim, J. Goyvaerts, B. Szelag, J. Fedeli, P. Absil, T. Aalto, M. Harjanne, C. Littlejohns, G. Reed, G. Winzer, S. Lischke, L. Zimmermann, D. Knoll, D. Geuzebroek, A. Leinse, M. Geiselmann, M. Zervas, H. Jans, A. Stassen, C. Domínguez, P. Muñoz, D. Domenech, A. L. Giesecke, M. C. Lemme, and R. Baets, "Open-access silicon photonics platforms in Europe," IEEE J. Sel. Top. Quantum Electron. **25**(5), 1–18 (2019).
5. Y. Shi, Z. Wang, J. V. Campenhout, M. Pantouvaki, W. Guo, B. Kunert, and D. V. Thourhout, "Optical pumped InGaAs/GaAs nano-ridge laser epitaxially grown on a standard 300-mm Si wafer," Optica **4**(12), 1468–1473 (2017).
6. S. Lin, X. Zheng, J. Yao, S. S. Djordjevic, J. E. Cunningham, J.-H. Lee, I. Shubin, Y. Luo, J. Bovington, D. Y. Lee, H. D. Thacker, K. Raj, and A. V. Krishnamoorthy, "Efficient, tunable flip-chip-integrated III-V/Si hybrid external-cavity laser array," Opt. Express **24**(19), 21454–21462 (2016).
7. D. Shin, J. Cha, S. Kim, Y. Shin, K. Cho, K. Ha, G. Jeong, H. Hong, K. Lee, and H.-K. Kang, "O-band dfb laser heterogeneously integrated on a bulk-silicon platform," Opt. Express **26**(11), 14768–14774 (2018).

Optics EXPRESS

8. J. M. Ramirez, H. Elfaiki, T. Verolet, C. Besancon, A. Gallet, D. Néel, K. Hassan, S. Olivier, C. Jany, S. Malhouitre, K. Gradkowski, P. E. Morrissey, P. O'Brien, C. Caillaud, N. Vaissiére, J. Decobert, S. Lei, R. Enright, A. Shen, and M. Achouche, "III-V-on-Silicon integration: From hybrid devices to heterogeneous photonic integrated circuits," IEEE J. Sel. Top. Quantum Electron. **26**(2), 1–13 (2020).
9. K. Van Gasse, R. Wang, and G. Roelkens, "27 db gain III-V-on-silicon semiconductor optical amplifier with> 17 dBm output power," Opt. Express **27**(1), 293–302 (2019).
10. J. Zhang, B. Haq, J. O Callaghan, A. Gocalinska, E. Pelucchi, A. J. Trindade, B. Corbett, G. Morthier, and G. Roelkens, "Transfer-printing-based integration of a III-V-on-silicon distributed feedback laser," Opt. Express **26**(7), 8821–8830 (2018).
11. J. Wu, Q. Dan, and S. Liu, "Effect of viscoelasticity of PDMS on transfer printing," in *2015 16th International Conference on Electronic Packaging Technology (ICEPT)*, (2015), pp. 759–764.
12. J. Goyvaerts, S. Kumari, S. Uvin, J. Zhang, R. Baets, A. Gocalinska, E. Pelucchi, B. Corbett, and G. Roelkens, "Transfer-print integration of gaas p-i-n photodiodes onto silicon nitride waveguides for near-infrared applications," Opt. Express **28**(14), 21275–21285 (2020).
13. B. Haq, S. Kumari, K. Van Gasse, J. Zhang, A. Gocalinska, E. Pelucchi, B. Corbett, and G. Roelkens, "Micro-transfer-printed III-V-on-Silicon C-Band semiconductor optical amplifiers," Laser Photonics Rev. **14**(7), 1900364 (2020).
14. J. Zhang, G. Muliuk, J. Juvert, S. Kumari, J. Goyvaerts, B. Haq, C. Op de Beeck, B. Kuyken, G. Morthier, and D. Van Thourhout, "III-V-on-Si photonic integrated circuits realized using micro-transfer-printing," APL Photonics **4**(11), 110803 (2019).
15. T. Komljenovic, M. Davenport, J. Hulme, A. Y. Liu, C. T. Santis, A. Spott, S. Srinivasan, E. J. Stanton, C. Zhang, and J. E. Bowers, "Heterogeneous silicon photonic integrated circuits," J. Lightwave Technol. **34**(1), 20–35 (2016).